

WHAT IS CLAIMED IS:

1. A method for isolating self-aligned contact pads of a semiconductor device, the semiconductor device including a first pattern having self-aligned contact holes and a second pattern, comprising:
 - 5 forming a test semiconductor device, the test semiconductor device having a first test pattern having self-aligned contact holes and a second test pattern, the first test pattern and the second test pattern being formed in the vicinity of a main pattern;
 - 10 measuring a step difference between the first test pattern and the second test pattern;
 - 15 performing a chemical mechanical polishing process on the test semiconductor device so as to isolate self-aligned contact pads formed in the self-aligned contact holes of the test semiconductor device;
 - 20 measuring a step difference between the first test pattern and the second test pattern after the chemical mechanical polishing process;
 - 25 setting a relationship equation among the step difference between the first test pattern and the second test pattern before the chemical mechanical polishing process, the step difference between the first test pattern and the second test pattern after the chemical mechanical polishing process, and an extent of isolation of the self-aligned contact pads formed in the test semiconductor device;
 - 30 measuring a step difference between the first pattern and the second pattern of the semiconductor device;
 - estimating an appropriate chemical mechanical polishing time corresponding to the measured step difference between the first pattern and the second pattern of the semiconductor device by referring to the relationship equation;
 - 35 performing a chemical mechanical polishing process on the semiconductor device for the estimated chemical mechanical polishing time so

as to isolate self-aligned contact pads formed in the self-aligned contact holes of the semiconductor device;

measuring a step difference between the first pattern and the second pattern of the semiconductor device after the chemical mechanical polishing process;

comparing the measured step difference between the first pattern and the second pattern of the semiconductor device after the chemical mechanical polishing step with a reference value, the reference value being a step difference necessary to achieve a desired extent of isolation of the self-aligned contact pads; and

correcting the chemical mechanical polishing time for sufficiently isolating self-aligned contact pads based on the comparison result.

2. The method of claim 1, wherein the relationship equation is set in consideration of a proportional relationship between the step difference between the first test pattern and the second test pattern before the chemical mechanical polishing process and chemical mechanical polishing time.

3. The method of claim 1, wherein the relationship equation comprises a proportional relationship between the step difference between the first test pattern and the second test pattern after the chemical mechanical polishing process and the extent of isolation of the self-aligned contact pads formed in the test semiconductor device.

4. The method of claim 1, wherein the first test pattern and the second test pattern have a same size and a same structure as those of the main pattern.

5. The method of claim 4, wherein the main pattern, the first test pattern, and the second test pattern comprise a gate insulating layer, a gate conductive layer, and a gate capping layer, which are sequentially stacked.

6. The method of claim 1, wherein before performing the chemical mechanical polishing process on the semiconductor device, a conductive layer is formed over the first pattern and the second pattern.

5 7. A method for isolating self-aligned contact pads of a semiconductor device, comprising:

is determining a chemical mechanical polishing process time necessary to isolate the self-aligned contact pads a desired amount by referring to a relationship equation between the extent of isolation of the self-aligned contact pads and the chemical-mechanical polishing process time;

10 performing a chemical mechanical polishing process for the determined process time on the semiconductor device to isolate the self-aligned contact pads the desired amount.

15 8. The method of claim 7, wherein the relationship equation is determined using a test semiconductor device.

9. The method of claim 7, further comprising:

etching the semiconductor device to form self-aligned contact holes.

20 10. The method of claim 9, further comprising:
forming a conductive layer over the self-aligned contact holes before performing the chemical mechanical polishing process.

25 11. A semiconductor device, comprising:
a first pattern having self-aligned contact holes and a second pattern; and
self-aligned contact pads formed in the self-aligned contact holes, wherein the semiconductor device is formed by a process comprising:

forming a test semiconductor device, the test semiconductor device having a first test pattern having self-aligned contact holes and a second test pattern, the first test pattern and the second test pattern being formed in the vicinity of a main pattern;

5 measuring a step difference between the first test pattern and the second test pattern;

 performing a chemical mechanical polishing process on the test semiconductor device so as to isolate self-aligned contact pads formed in the self-aligned contact holes of the test semiconductor device;

10 measuring a step difference between the first test pattern and the second test pattern after the chemical mechanical polishing process;

 setting a relationship equation among the step difference between the first test pattern and the second test pattern before the chemical mechanical polishing process, the step difference between the first test pattern and the second test pattern after the chemical mechanical polishing process, and an extent of isolation of the self-aligned contact pads formed in the test semiconductor device;

15 measuring a step difference between the first pattern and the second pattern of the semiconductor device;

20 estimating an appropriate chemical mechanical polishing time corresponding to the measured step difference between the first pattern and the second pattern of the semiconductor device by referring to the relationship equation;

 performing a chemical mechanical polishing process on the semiconductor device for the estimated chemical mechanical polishing time so as to isolate self-aligned contact pads formed in the self-aligned contact holes of the semiconductor device;

25 measuring a step difference between the first pattern and the second pattern of the semiconductor device after the chemical mechanical polishing process;

comparing the measured step difference between the first pattern and the second pattern of the semiconductor device after the chemical mechanical polishing step with a reference value, the reference value being a step difference necessary to achieve a desired extent of isolation of the self-aligned contact pads; and

correcting the chemical mechanical polishing time for sufficiently isolating self-aligned contact pads based on the comparison result.

12. The semiconductor device of claim 11, wherein the relationship
10 equation is set in consideration of a proportional relationship between the step difference between the first test pattern and the second test pattern before the chemical mechanical polishing process and chemical mechanical polishing time.

13. The semiconductor device of claim 11, wherein the relationship
15 equation comprises a proportional relationship between the step difference between the first test pattern and the second test pattern after the chemical mechanical polishing process and the extent of isolation of the self-aligned contact pads formed in the test semiconductor device.

20 14. The semiconductor device of claim 11, wherein the first test pattern and the second test pattern have a same size and a same structure as those of the main pattern.

25 15. The semiconductor device of claim 14, wherein the main pattern, the first test pattern, and the second test pattern comprise a gate insulating layer, a gate conductive layer, and a gate capping layer, which are sequentially stacked.

16. The semiconductor device of claim 11, wherein before performing the chemical mechanical polishing process on the semiconductor device, a conductive layer is formed over the first pattern and the second pattern.